International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 4 Issue 10 ǁ October. 2016 ǁ PP.60-66

Design of 600-800 MHz Programmable Phase Locked Loop

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Abstract: In this paper – emphasis is made on the design and architecture of the Programmable PLL. The frequency range of working of the Programmable PLL is 600-8000MHz with settling times 9, 10, 13 and 20 uSec for the frequencies 600,700,750 and 800 MHz respectively. The programmable PLL is obtained by designing a Programmable frequency divider which has four scale down factors to obtain the desired frequency. The Proposed circuit is designed in 180nm, 3.3 V CMOS technology and simulated using Cadence Virtuoso simulator. There are mainly five parts in the Programmable PLL. They are Phase Detector (PD), Charge Pump (CP), Loop Filter (LP) Voltage control oscillator (VCO) and Programmable frequency divider.
Keywords: programmable PLL, phase detector, voltage control oscillator, charge pump, frequency divider.

I. INTRODUCTION

As the communication technology progresses, the requirement of higher speed lock-up time, smaller size and, low power consumption PLL synthesizers have become crucial in the field of PLL Design. Various procedures and methods have been proposed to attain a high speedlock-up time in a PLL frequency synthesizer[1-4].Loop gain of the PLL has become an important and crucial parameter in PLL design. Many architectures have been proposed in order to increase the loop gain and to achieve a high speed lock-up time of PLL frequency synthesizers[5-6]. For example, the fractional division method has been implemented to increase the loop gain[7,8]. However, in proposed method the usage of two different division ratios alternately have been implemented, the phase noise caused the more spurious noise around the reference frequency even though the loop is in steady state condition. In a conventional PLL, once theprogrammable divider or phase detector is chosen as an element of the PLL[9], the loop gain of PLL becomes fixed. In this paper, we propose a new PLL frequency synthesizer with multi-programmable divider which can attain a higher speed lock-up time.

Phase locked loop is a circuit which synchronizes the output frequency with the input reference frequency signal. Programmable PLL consists of mainly five parts. They are Phase Detector (PD), Charge Pump (CP), Loop Filter (LP), Voltage Control Oscillator (VCO) and Programmable Frequency Divider.

2. Dynamics of Charge Pump PLL

In order to enumerate the behavior of charge-Pump PLL a linear model has to be implemented for the combination of the PFD, charge pump and the low-pass filter so as to obtain the transfer function of the combination[8]. From the observations of the output of the loop filter we can express as

$$V_{out}(t) = \frac{I_P}{2\pi C_P}\, t.\emptyset_0 u(t) \quad (1.0)$$

The impulse response of the system is given by eq.1.1

$$h(t) = \frac{I_P}{2\pi C_P} u(t) \quad (1.1)$$

The transfer function is given by the following expression

$$\frac{V_{out}}{\Delta\emptyset}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{S} \quad (1.2)$$

From the above transfer function we can observe that the combination of the PFD/CP/LPF contains a pole at the origin. In analogy, $I_P/2\pi C_P$ is expressed as the gain of the PFD and denoted as K_{PFD}. The linear model of the charge-pump PLL can be constructed as shown in Figure1.and the model gives an open-loop transfer function is given by eq.1.3

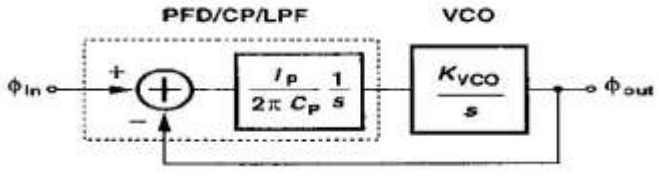

Figure 1. Linear model of Charge Pump PLL

$\frac{\emptyset_{out}}{\emptyset_{in}}(s)|open = \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{S^2}$ (1.3)

Since from the above transfer function it is observed that there are two poles at the origin, Thistype of topology is called a "type II" PLL. The closed loop transfer function is denoted by H(s) for the sake of brevity, is thus equal to

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}}{S^2+\frac{I_P K_{VCO}}{2\pi C_P}} \quad (1.4)$$

The result of the transfer is alarming due to the presence of the imaginary poles at $S_{1,2} = \pm j\sqrt{I_P K_{VCO}/2\pi C_P}$ which makes the loop unstable. The instability of the loop is due to the presence of the poles at the origin which are seen from the open loop of the transfer function of the linear-model. The presence of each pole adds an additional phase of 90^0, allowing tooscillate at the gain crossover frequency. In order to stabilize the loop we need to modify the phase of the system which can reduce the 180^0 phase shift at the gain cross over frequency which is possible by introduction of the zero in the loop gain. This is done by introduction of the resistor in series with the loop filter capacitor which then modifies the PFD/CP/LP transfer function to expression 1.5

$$\frac{V_{out}}{\Delta\emptyset}(s) = \frac{I_P}{2\pi}\left(R_p + \frac{1}{C_{ps}}\right) \quad (1.5)$$

The open-loop transfer function of the Charge pump PLL is given by eqn.1.6

$\frac{\emptyset_{out}}{\emptyset_{in}}$(s)|open = $\frac{I_P}{2\pi}\left(R_p + \frac{1}{C_{ps}}\right)\frac{K_{VCO}}{S}$ (1.6)

And hence

$$H(S) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_p C_{ps}+1)}{S^2+\frac{I_P}{2\pi}K_{VCO} R_p S+\frac{I_P}{2\pi C_P}K_{VCO}} \quad (1.7)$$

The closed loop system contains a zero at S_z= -1/ $(R_p C_p)$. Using the same notation as that for the type I PLL, we have

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \quad (1.8)$$

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_P C_p K_{VCO}}{2\pi}} \quad (1.9)$$

3. Components of PLL

The various components of the programmable PLL are Phase detector (PD),Charge Pump (CP), Loop Filter (LP) Voltage Control Oscillator (VCO) and Programmable Frequency Divider. The brief description of each component is given below.

3.1 Phase Detector

Phase detector is a module which produces output signals which is proportional to the phase of the input signals. The PD has namely two output signals UP and DOWN and the input signals are input reference signal and the output of the Programmable frequency divider. The architecture of the PD is depicted in Figure2.

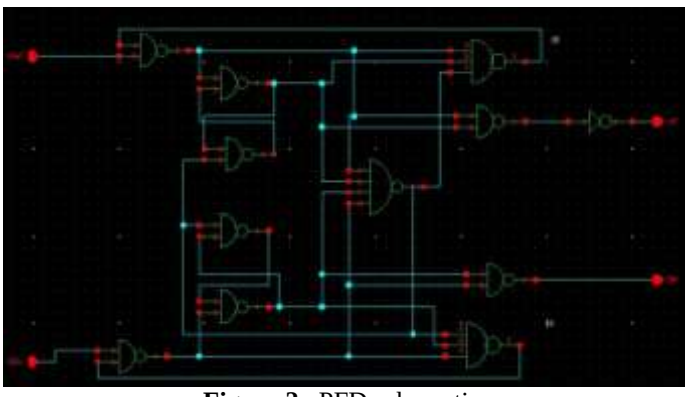

Figure 2. PFD schematic

3.2 Charge Pump

The Charge Pump can be modeled as transconductive device which convert the Phase difference of the input signals into the current. The circuit diagram of the charge Pump is depicted in Figure3.

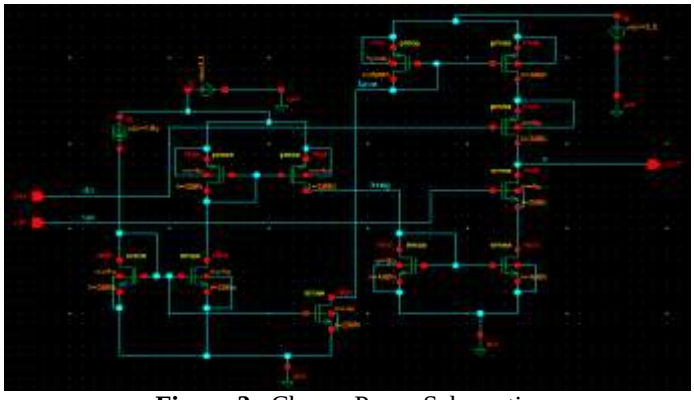

Figure 3. Charge Pump Schematic

3.3 Loop filter

The function of the loop filter is to eliminate the unwanted high frequency signal and to integrate the DC voltage signal to the VCO. The Loop filter is designed using the following values in the table and by simulation of the eq.1.7 in the MATLAB environment and the values of the R and C are evaluated. The third order loop filter is depicted in Figure4.and the parameters considered while designing the loop filter are tabulated in the Table 1.

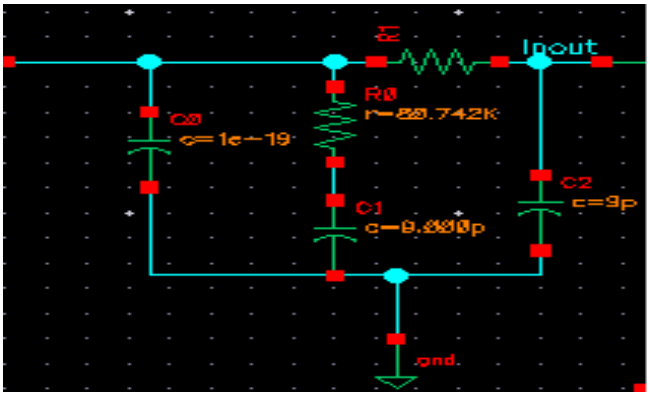

Figure 4. Loop Filter

Table 1. Parameters used in designing of the Loop Filter

Output frequency	800MHz
Input reference frequency	25MHz
Phase Margin	70^0
VCO gain	300 MHz/V
Charge Pump current	10uA
Filter Bandwidth	2MHz

3.4 Voltage Controlled Oscillator (VCO):

VCO works on the principle of the 'Barkhausen Criteria'. It states that "The frequency of oscillation at which sinusoidal oscillator operates is the frequency for which the total shift introduced, as the signal proceeds from the input terminals, through the amplifier and feedback network, and back again to the input, is precisely zero(or an integral multiple of 2*Π)(Or)Stated simply the condition $A*\beta = -1$ at $\omega = \omega_o$, i.e. the magnitude of loop gain should be one and phase of loop gain should be unity (the feedback network introduces 180^0 phase shift, the other 180^0 phase shift is provided by mixer) is called Barkhausen criterion". In VCO[10] the frequency of oscillation is varied by the applied input DC voltage. When there is no input voltage, the output of the VCO will have a frequency called "free oscillation frequency".It has an integratorfunction for the phase input signal. VCO which is designed in the present work is using the differential- ring oscillator. The gain of the VCO is denoted by K_{VCO} and the gain of the K_{VCO} designed is about 300MHz/V. The Figure5.depicts the schematic

design of VCO which has 1V as controllable voltage and the output frequency is 600-800Mhz range and the gain of the VCO which is denoted by K_{VCO} graph is depicted in Figure6.

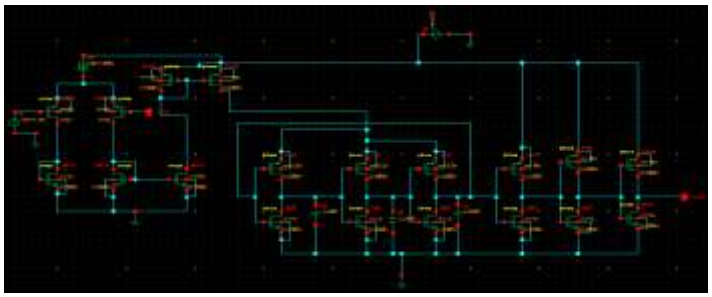

Figure 5. VCO schematic

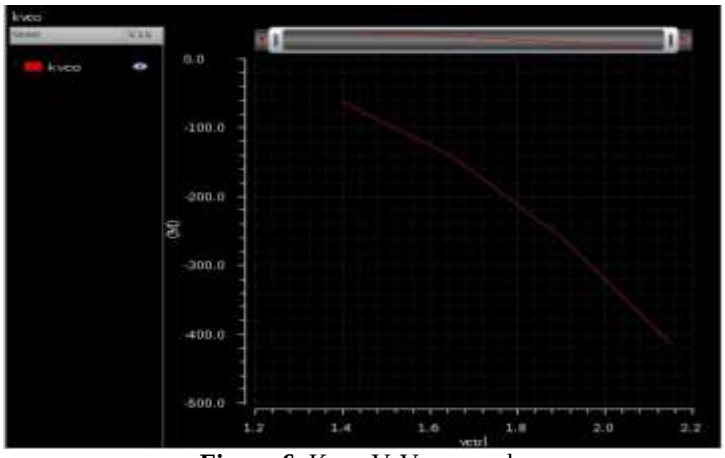

Figure 6. K_{VCO} $V_S V_{Ctrl}$ graph

3.5 Programmable Frequency Divider

The Programmable frequency divider has two control inputs S1 & S0 to select the predefined customized frequencies. In this the frequency of the VCO is scaled down. The amount by which the frequency is scaled down is multiplied with the input reference frequency. The principle used here is

$f_{out} = N \times f_{ref}$ (1.10)

Where N is the scale down factor in the frequency divider. When 'S1S0' is '00', '01', '10' and '11' the frequencies are scaled down by 24,28,30 and 32 whereas the output frequency of the PLL obtained is 600,700,750 and 800MHz respectively. The schematic of the programmable frequency divider is depicted in the Figure 7.

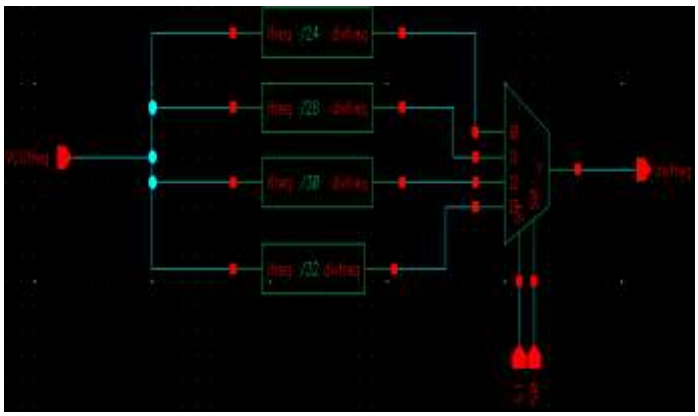

Figure 7. Programmable frequency divider.

II. Discussion

The outputs of the programmable PLL for different input combination of 'S_1S_0' of frequency divider are depicted in the following Figures 8-15. When 'S_1S_0' is '00' the output frequency of the PLL obtained is 600

MHz. Similarly when 'S_1S_0' is '01','10'and '11' the output frequency of the PLL is 700,750 and 800MHz respectively. The Lock time and the power consumption for each frequency are summarized in Table 2.

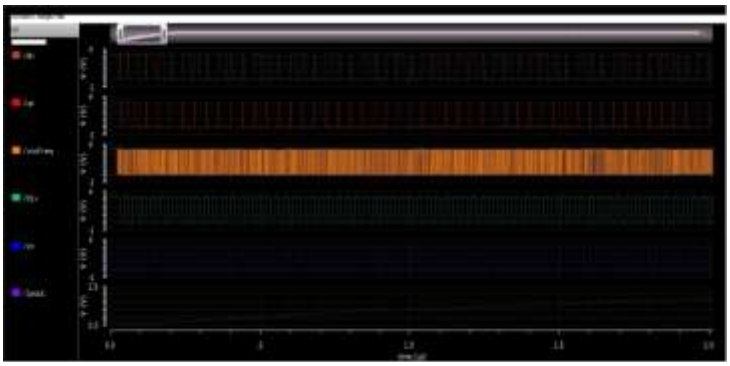

Figure 8. Various outputs of PLL structure for 600MHz

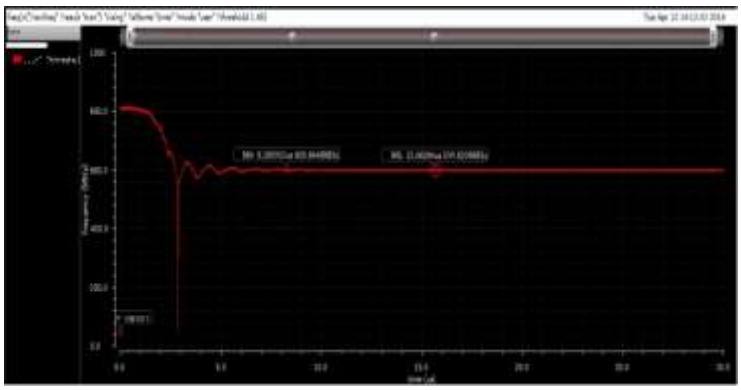

Figure 9. Settling frequency of PLL structure for 600MHz

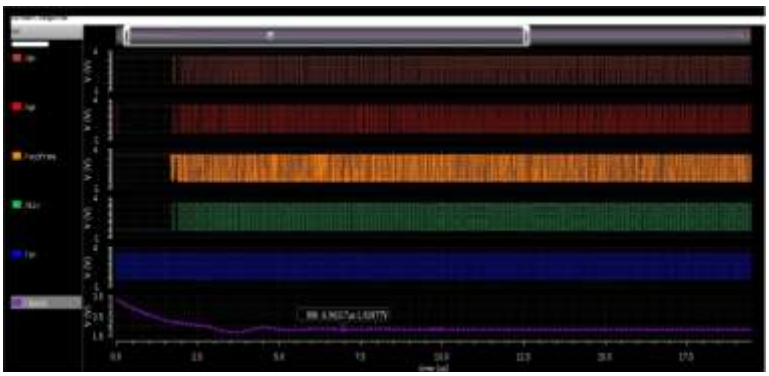

Figure 10. Various outputs of PLL structure for 700MHz

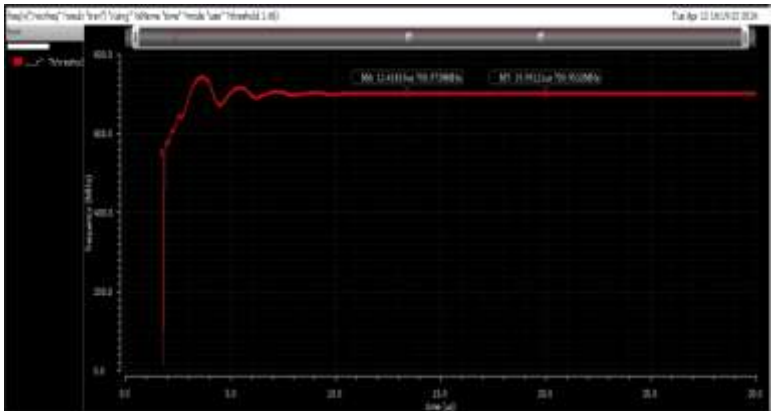

Figure 11. Settling frequency of PLL structure for 700MHz

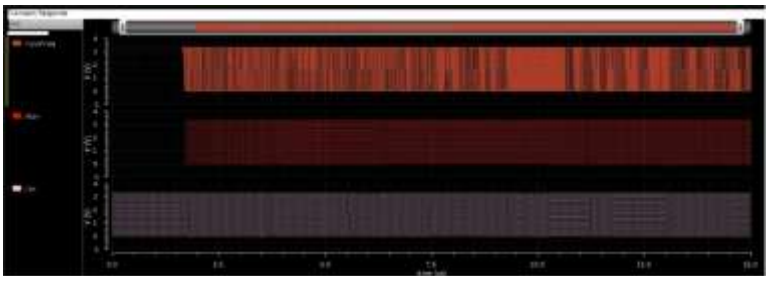

Figure 12. Various outputs of PLL structure for 750MHz

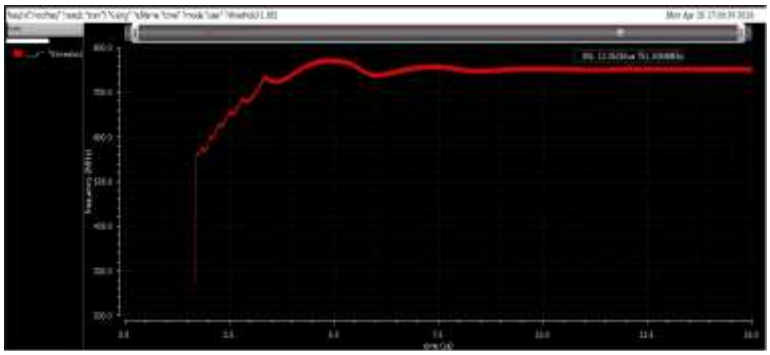

Figure 13. Settling frequency of PLL structure for 750MHz

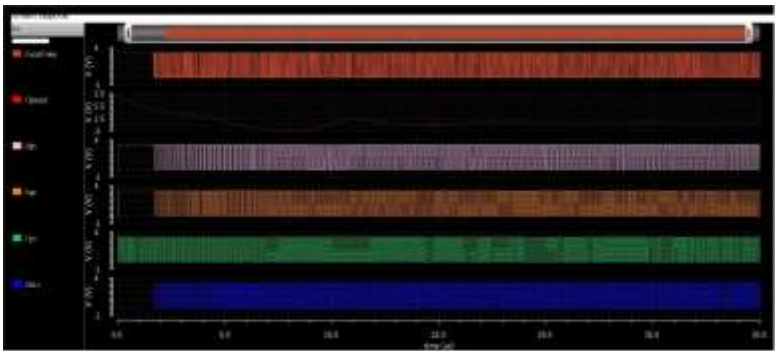

Figure 14. Various outputs of PLL structure for 800MHz

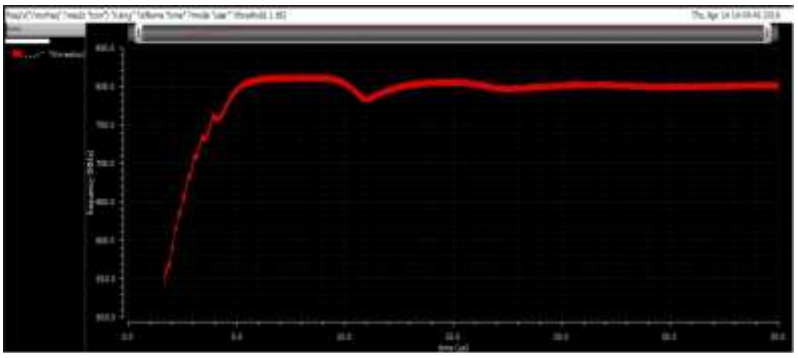

Figure 15. Settling frequency of PLL structure for 800MHz

Table 2. Lock time and Power consumption of the PLL for 600-800 Mhz

Selection input	**Frequency in MHz**	**Lock time in µS**	**Power consumption(Watt)**
00	600	9	12.5m
01	700	10	2.3
10	750	13	2.16
11	800	20	1.98

III. Conclusion

In this paper, we have designed and simulated the programmable PLL structure has been done. The variation of the Lock time with the Frequency of oscillation is observed and also the power consumption at various frequencies is calculated. The Design and simulation of the whole structure is done in Cadence Virtuoso environment. The Proposed circuit is designed in 180nm, 3.3 V CMOS technology. The frequency range of the PLL is 600-800MHz and different precustomized frequencies in the range can be selected with S_1 &S_0inputs. The lock time of the circuit varied from 9 to 20 µS with variation of the frequency from 600 to 800MHz.

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